FLIP FLOP, SHIFT REGISTER, AND OPERATING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a flip flop used for general ICs and a shift register composed of a plurality of flip flops which are connected thereto.

2. Description of the Related Art

Fig. 5 shows an example of a conventional flip flop.

This flip flop is composed of transmission gates as a switching elements, inverters, and latch elements. In a general standby state, an S terminal is set to a high state and an SX terminal is set to a low state, so that an M terminal is held in a high state and a QX terminal is held in a low state.

Fig. 6 shows a shift register composed of a plurality of flip flops as described above which are connected in series.

However, there is a problem in that a large number of elements are used for such a flip flop.

Also, in the shift register composed of the plurality of flip flops that are connected in series, signal lines for the S terminal and the SX terminal are required. Therefore, it is necessary to use four signal lines including signal lines for a C terminal and a CX terminal.

Thus, there is a problem in that a layout area is large.

SUMMARY OF THE INVENTION

A flip flop according to the present invention includes: a first switching element in which a first terminal thereof is connected with a data input terminal; a first inverter element in which an input terminal thereof is connected with a second terminal of the first switching element; a second switching element in which an output of the first inverter element is inputted to a first terminal thereof; and a second inverter element in which an input terminal thereof is connected with the second terminal of the second switching element. Further, the flip flop is characterized in that an output terminal of the second inverter element is a data output terminal.

According to the flip flop of the present invention, a transistor for maintaining a standby state is unnecessary, so that a layout area can be decreased. In addition, in the shift register composed of the plurality of flip flops connected in series, common signal lines for bringing the shift register to the standby state are unnecessary, so that the layout area can be decreased.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Fig. 1 is a circuit diagram of a flip flop of the present invention;

Fig. 2 shows an example of a circuit for making signals CX and C supplied to the flip flop of the present invention;

Fig. 3 is a timing chart showing operation of the flip flop of the present invention;

Fig. 4 is a circuit diagram of a shift register composed of a plurality of flip flops of the present invention which are connected in series;

Fig. 5 is a circuit diagram of a conventional flip flop; and

Fig. 6 is a circuit diagram of a conventional shift register.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, the present invention will be described with reference to the drawings.

Fig. 1 is a circuit diagram of a flip flop of the present invention.

This flip flop includes an NMOS transistor 1 as a first switching element, a first inverter 2, an NMOS transistor 3 as a second switching element, a second inverter 4, and transistors 5 and 6 as latch elements. Because the flip flop is composed of two switching elements, two inverters, and two

transistors, the number of elements can be made small. In addition, if potentials on an M terminal and a QX terminal are stable, the latch elements 5 and 6 can be omitted.

Fig. 2 shows an example of a circuit for producing signals CX and C that are inputted to the gates of the switching elements 1 and 3 in the flip flop. According to this circuit, when RX is in a low state, the signals C and CX always become a high state.

Fig. 3 is a timing chart showing operations of the circuit shown in Figs. 1 and 2.

When RX is in the low state, the signals C and CX are at the high level, so that the switching elements 1 and 3 are turned ON. Therefore, all potentials in the flip flop are fixed. When D is in the low state, M and Q are fixed to the low state and MX and QX are fixed to a high state. When D is in the high state, M and Q are fixed to the high state and MX and QX are fixed to the low state. In other words, because there is no unsteady potential, a reliable standby state is obtained. When RX becomes the high state, the signal C becomes an inverted pulse of CLK and the signal CX becomes a pulse in phase with CLK, so that data transfer is possible.

Fig. 4 is a circuit diagram of a shift register composed of a plurality of flip flops of the present invention which are connected in series. This shift register is composed of

the flip flops shown in Fig. 1 and the signals C and CX are supplied from the circuit shown in Fig. 2. Accordingly, in the standby state, all Q outputs are fixed to the low state or the high state.

Common signal lines of the shift register are provided for only the signals C and CX, and common signal lines for bringing the shift register to the standby state are unnecessary. In other words, common lines composing the shift register are a power source line and two lines for the signals C and CX, so that the layout area can be decreased.

In the above description, the first switching element or the second switching element may be a transmission gate or a PMOS transistor.

As described above, according to the flip flop of the present invention, a transistor for maintaining to a standby state is unnecessary, so that a layout area can be decreased. In addition, in the shift register of the present invention, common signal lines for bringing the shift register to the standby state are unnecessary, so that the layout area can be decreased.